DESIGN AND ANALYSIS OF COMPRESSOR-BASED AREA-EFFICIENT, HIGH-SPEED LOW-POWER MULTIPLIER

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ABSTRACT- *Multiplication is the basic arithmetic operation that is important in several microprocessors and digital signal-processing applications. Microprocessors use multipliers within their arithmetic logic units, and digital signal processing systems require multipliers to implement DSP algorithms such as convolution and filtering. Multipliers being the most area and power-consuming elements of a design, area-efficient low-power multiplier architectures are in demand. In this paper, a multiplier based on an ancient Vedic mathematics technique has been proposed which employs 4:3, 5:3, 6:3, and 7:3 compressors for the addition of partial products. Combining the Vedic multiplier and efficient compressors, a robust area and power-efficient multiplier architecture has been achieved. The designs were synthesized and analysed in Cadence Virtuoso in 180 nm technology. When compared with the previous compressor-based multiplier, the proposed design achieves a reduction in power and area respectively.*

Index Terms— *Half adder, Full adder, compressor, Vedic multiplier, Low-power and High-speed*

I. INTRODUCTION

Multipliers are the key components of all digital signal processors (DSPs), FIR filters, and image processors, and the performance of these processors is largely determined by the kind of multipliers used. They are generally the most area-consuming and hence power power-consuming units in the design. Therefore, optimizing the area and power of the multiplier is a major design issue.
Several multipliers have been proposed and designed over the past few decades [1]. In these algorithms, the multiplication process requires several intermediate stages to get the final result due to which the critical path gets lengthened. Also, these intermediate stages require additional hardware which leads to an increase in area and power consumption.
To overcome these disadvantages, multipliers based on the Vedic technique have been proposed in [2] and [3] where all the partial products are obtained well in advance much before the actual operation of multiplication begins, which results in a speed design.
In this paper, a novel multiplier architecture is proposed that can efficiently reduce the intermediate stages as compared to a compressor-based multiplier by using high-order compressors such as 4:3, 5:3, 6:3, and 7:3 compressors [5]

Section II explains the high-order compressors used in this paper. Section III describes the Vedic technique for 8-bit multiplication. Section IV describes the proposed multiplier. Section V discussion conclusion

II. HIGHER-ORDER COMPRESSORS

Several 4-2 and 5-2 compressor architectures have been reported so far [5] and [6]. The main drawback associated with these conventional compressors is that the result generated is not in proper binary form and one more half adder/ full adder is required to get the final results, thereby increasing the area and power dissipation. Moreover, due to uneven delay profiles of the outputs arriving from different input paths, a lot of glitches are generated. To overcome these problems associated with the

conventional compressors, higher-order compressors proposed in [7] have been used in the design. These compressors have been designed as counters of 1's at the input bits. Full adder itself is a counter of 1's at its input as illustrated in Table I. Therefore, a full adder acts as a 3-2 compressor. A similar logic can be used to design the higher-order compressor circuits.

Table I Full adder as a counter

Number of 1's at the input	Output		Equivalent decimal value
	Carry	Sum	
Zero	0	0	0
One	0	1	1
Two	1	0	2
Three	1	1	3

The concept of the 4-3 compressor as a counter is shown in Table II. Similarly, 5-3, 6-3, and 7-3 compressors can be obtained.

Table II 4-3 compressor as a counter

Number of 1's at the input	Output			Equivalent decimal value
	C3	C2	C1	
Zero	0	0	0	0
One	0	0	1	1
Two	0	1	0	2
Three	0	1	1	3
Four	1	0	0	4

The block diagram of 4-3, 5-3, 6-3 and 7-3 compressors are shown in Fig. 1, 2, 3, and 4 respectively.

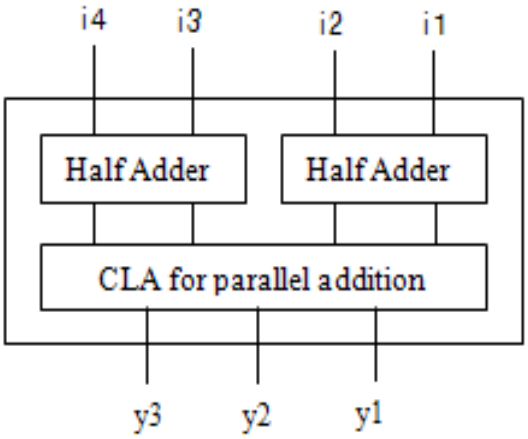

Fig.1. Block diagram of a 4-3 Compressor

The block diagrams of 4-3, 5-3 and 6-3 compressor contains three sub-units: two adder units and a Carry Look Ahead adder (CLA) unit for parallel addition of the outputs of the adder units. The 7-3 compressor is implemented using 4-3 compressor, a full adder and a CLA unit.

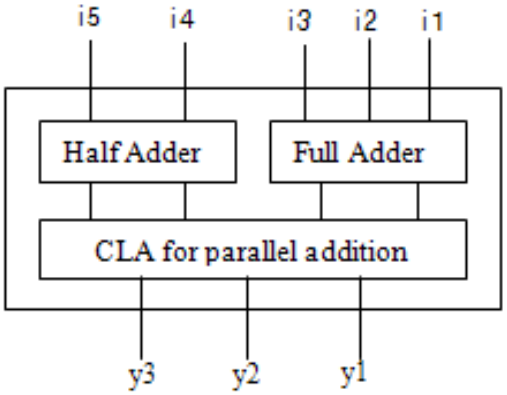

Fig.2. Block diagram of a 5-3 Compressor

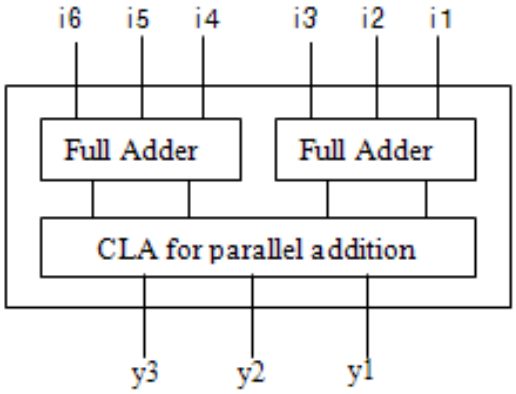

Fig.3. Block diagram of a 6-3 Compressor

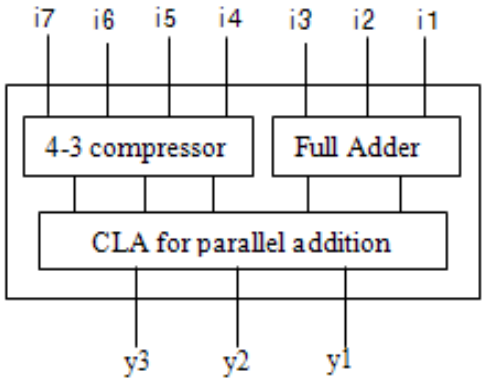

Fig.4. Block diagram of a 7-3 Compressor

III. HIGHER-ORDER COMPRESSOR BASED VEDIC MULTIPLIER

In the conventional Wallace Tree multiplier, the partial products are formed by AND gates in the same manner as that of the Dadda multiplier. The formed partial products are collected into groups of three or two. Full adders are applied to columns containing three bits and half adders to columns containing two bits. Carry-save adders are used for the addition of partial products [8]. Since the Wallace multiplier performs the reduction as soon as possible the number of half adders and full adders required is high. The conventional Wallace multiplier for 8-bit is shown in Figure 5.

In the earlier compressor-based Vedic Multiplier [4], a large number of stages are required to add the partial products to obtain the final results. The 4-2 and 7-2 compressors are utilized only in the first two stages of the multiplier. In contrast, the following eleven stages employ only full adder and half adder thereby increasing the reduction stages to thirteen. This leads to increased area and power consumption.

In the proposed multiplier architecture, the higher order compressors have been used intelligently so that the partial products are added in only two stages to obtain the final result hence giving an area efficient and low power consuming design. Also, compressors and adders are employed such that a

minimum number of outputs is generated. For example in column 5, there are 7 partial products to be added. These could be added using a 4-3 compressor and a full adder thereby generating five output bits. But instead of this a 7-3 compressor has been used which will generate only 3 output bits. The same approach has been utilized for other columns as well. The dot diagram of the proposed multiplier is shown in Fig. 5

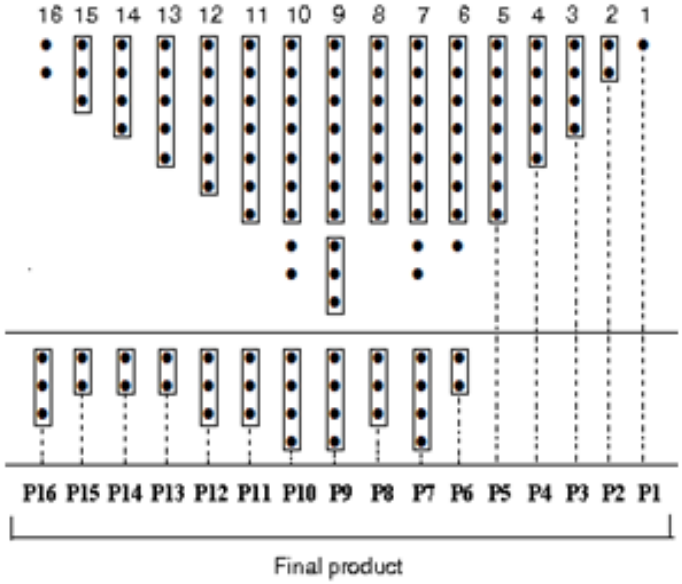

Fig.5. Dot Diagram of 8X8 multiplier

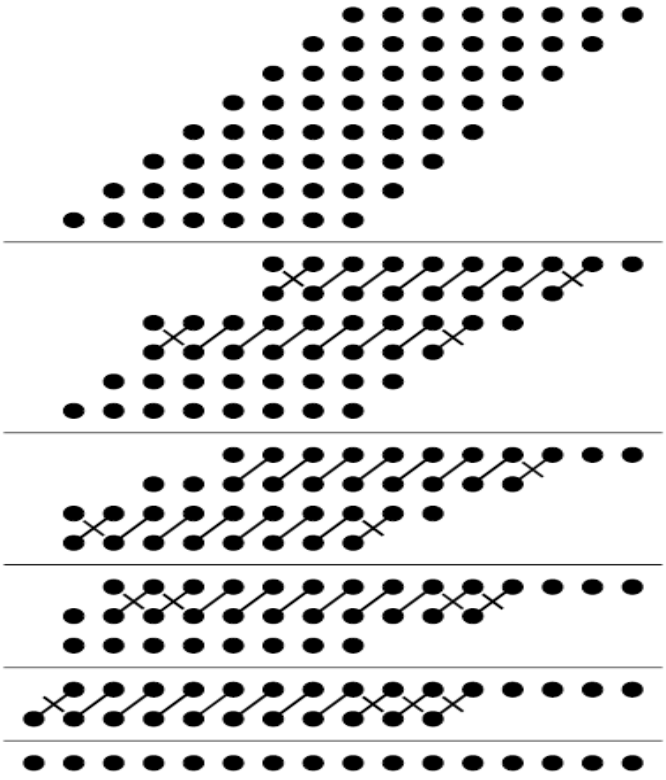

Figure 6. Wallace Multiplier for 8-bit

IV. MULTIPLIER PERFORMANCE AND COMPARISON

For performance comparison, various multipliers, conventional compressor-based Vedic multiplier, and the proposed higher-order compressor-based Vedic multiplier and Dadda have been implemented in Cadence virtuoso 180nm technology.

The design of an 8x8 multiplier for each of these architectures was simulated and synthesized in Cadence Virtuoso in 180 nm technology. The unoptimized gate count, area, and power have been compared.

V. CONCLUSION

In this paper, various higher-order compressors have been utilized to design an 8x8 multiplier. The performance of compressor-based Vedic multiplier and higher order compressor-based multiplier has been compared in terms of gate count, area, and power dissipation.
The use of higher-order compressors reduces the number of computational stages; thereby requiring less hardware. Hence the proposed design achieves a significant reduction in area, leakage power, dynamic power, and total power dissipation. The proposed Vedic multiplier architecture using higher-order compressors can be used in area and power-critical applications.

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