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A Review of an Efficient 8-bit Vedic Multiplier using Reversible Logic

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***Abstract*: This paper basically emphasizes on different methodologies that have been proposed from past few years on multiplier. Research on multiplier and reversible logic has widely covered applications such as design of ALU, RISC, CISC, Design of low power arithmetic and data path for digital signal processing (DSP), Low power CMOS, Optical computing, Quantum computing, Nanotechnology and many more .These applications led to untiring efforts for further techniques yet to be proposed. This paper enlightens us about numerous techniques that have extensively being used for Vedic multiplier based Nikhil am sutra using reversible logic.**

***Keywords*:**-Multiplier, Nikhilam sutra algorithm, Vedic multiplier, Xilinx, FPGA**.**

I. INTRODUCTION

Arithmetic operations such as addition, subtraction and multiplication are deployed in various digital circuits to speed up the process of computation. Arithmetic logic unit is also implemented in various processor architectures like RISC, CISC etc., In general, arithmetic operations are performed using the packed-decimal format. This means that the fields are first converted to packed-decimal format prior to performing the arithmetic operation, and then converted back to their specified format (if necessary) prior to placing the result in the result field.

Vedic mathematics has proved to be the most robust technique for arithmetic operations. In contrast, conventional techniques for multiplication provide significant amount of delay in hardware implementation of n-bit multiplier. Moreover, the combinational delay of the design degrades the performance of the multiplier. Hardware-based multiplication mainly depends upon architecture selection in FPGA or ASIC.

In this paper the section I provide the Introduction to Vedic multiplier and Reversible logic. Section II provides abrupt introduction to Vedic sutras. Section III Introduction of Reversible logic Section IV Literature survey. Section V represents the conclusion.

II. VEDIC SUTRAS

In Sanskrit, the word Sutra means "Thread of Knowledge". Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Application of the Sutras saves a lot of time and effort in solving the problems, compared to the formal methods presently in vogue. The application of the Sutras is perfectly logical and rational. The Sutras provide not only methods of calculation, but also ways of thinking for their application.

Application of the Sutras to specific problems involves rational thinking, which, in the process, helps improve intuition that is the bottom - line of the mastery of the mathematical geniuses of the past and the present such as Aryabhatta, Bhaskaracharya, Srinivasa Ramanujan, etc.

"Vedic mathematics" is comprised of sixteen main sutras and 13 sub sutras of simple mathematical formulae from the Vedas [15].

Table 2.1:16 Main Sutras in Vedic Mathematics

Ekadikena Purvena(also a corollary)	By one more than the one before
Nikhilam Navatascaramam Dasatah	All from 9 and the last from 10
Urdhva-tiryakbhyam	Vertically and Cross-Wise
Paravartya Yojayet	Transpose and Apply
Sunyam Samyasamuccaye	The summation if equal to Zero
(Anurupye) Sunyamanyat	If One is in Ratio the Other is Zero
Sankalana - vyavakalanabhyam	By Addition and by Subtraction
Purnapurnabhyam	By the Completion or Non-Completion
Chalana-Kalanabhyam	Sequential Motion
Yavadunam	The Deficiency
Vyastisamastih	Whole as One and One as Whole
Sesanyankena Caramena	The Remainders by the Last Digit
Sopantyadvayamantyam	The Ultimate and Twice the Penultimate
Ekanyunena Purvena	By One Less than the Previous One
Gunitasamuccayah	The Whole Product is the same
Gunakasamuccayah	Collectivity of multipliers

III. REVERSIBLE LOGIC

Physical reversibility [10] signifies a process that dissipates no energy to heat and logical reversibility states that earlier state of a process is ascertainable from the backward computation of a state at any given point of time. Complete physical reversibility is attainable only when the process is logically reversible [11]. Computation processes that erase information bits are irreversible.

In 1961 Landauer [1] specified that every time a bit of information is lost equivalent physical entropy is generated. This generated entropy will be transformed into heat as basics laws of thermodynamics say that entropy cannot be destroyed merely [11]. In accordance with Landauers principle one bit of information loss generates KTln2 joule of heat energy where K is Boltzmann constant and T is the operating temperature in Kelvin scale. In room temperature erasure of one bit information gives off negligible amount of heat but large amount of heat generated as result of huge amount of information loss in high speed operation that engages more operational bits has serious effect on device performance and durability of components.

As predicted in Moore's law we found exponential increment in computer speed and power dissipation due to integration of enormous components in minimized area. This refinement of technology is bounded by lots of fundamental limits that are governed by well-established fundamental laws of physics and are technology independent [11]. At this point low power technologies may find its interest in quantum computing as an alternative to sustain the development flow. Quantum computation is based on unitary transformations that are reversible [12]. In 1973 C. H. Bennett [4] revealed that energy dissipation in a circuit can be avoided completely if the circuit is made up of reversible logic gates. So, reversible logic will play an important role in future technology [28].

To implement reversible computation, estimate its cost, and to judge its limits, it is formalized it in terms of gate level circuits. Reversible computing will also lead to improvement in power efficiency. Power efficiency will fundamentally affect the speed of circuits such as nano circuits— and therefore the speed of most computing applications. [11]

Design parameters of reversible logic circuits:

A. Quantum Cost: Quantum Cost of the circuit is considered by knowing the number of simple reversible gates (gates of which rate is previously identified) needed to realize the circuit.

B. Garbage Output: The output of the reversible gate that is not used as a main output or as input to other gates is called the garbage output. In little the unexploited output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are required in the circuit to retain the reversibility concept. [11]

C. Constant Inputs: The proposed reversible full adder gate requires only one constant input and it is theoretically minimum.

D. Gate count: Total number of reversible logic gates used to implement the intended logic circuit.

E. Total Reversible Logic Implementation Cost (TRLIC) [11]: This refers to the summation of gate count, constant inputs, garbage outputs and quantum cost of the circuit.

Design Constraints for Reversible Logic Circuits:

The following are the important design constraints for reversible logic circuits [4].

1) Reversible logic gates do not allow fan-outs.
2) Reversible logic circuits should have minimum quantum cost.
3) The design can be optimized so as to produce minimum number of garbage outputs.
4) The reversible logic circuits must use minimum number of constant inputs.
5) The reversible logic circuits must use a minimum logic depth or gate levels.

Reversible Logic Gates:

1) The Not gate: the only gate from conventional logic that is reversible.

2) Feynman Gate [6]: It is 2x2 gates. If the first input i.e. A Is given as 1 the second output will be the complement of the Second input i.e. B. so, this gate is also known as Controlled Not Gate. It can also be used to copy inputs. Quantum cost of this gate is one.

3) Peres Gate [7]: It is a 3x3 gate. It can be used as a half adder with third input i.e. c as 0.It also serves the purpose of fan out. Quantum cost of this gate is four.

4) Toffoli gate [5], or controlled-controlled-not gate, negates the input A if and only if both controls C1 and C2 are true.

4) HNG Gate [14]: It is a 4x4 gate. A single HNG gate can serve as a one bit full adder. Quantum cost of this gate is six.

5) BVPPG gate: In [23] this 5x5 reversible gate is proposed. It is basically for multiplication and can generate two partial products at a time. Quantum cost of this gate is ten.

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

1) Low power CMOS
2) Optical computing
3) Quantum computer
4) Nanotechnology
5) Design of low power arithmetic and data path for digital signal processing (DSP)
6) Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

IV. LITERATURE SURVEY

Multiplier implementation has already been reported using different multiplier architectures.

N. Ravi Research scholar (SVU), et all "A New Design for Array Multiplier with Trade off in Power and Area". In this paper a low power and low area array multiplier with carry save adder is proposed. The adder eliminates the final addition stage of the multiplier. In this paper, The proposed 4x4 multiplier to add carry bits without using Ripple Carry Adder (RCA) in the final stage, the carries given to the input of the next left column input.[17] The array multiplier, has high operational speed but it consumes more power with high requirement of space to implement large number of components required. [13]. Major limitation of array multiplier is its size. As operand sizes increase, arrays grow in size at a rate equal to the square of the operand size.

Shaik. Kalisha Baba "Design and Implementation of Advanced Modified Booth Encoding Multiplier". This paper presents Booth Encoder circuit generates half the partial products in parallel. By extending sign bit of the operands and generating an additional partial product the AMBE multiplier is obtained. The Carry Save Adder (CSA) tree and the final Carry Look ahead (CLA) adder used to speed up the multiplier operation. If we observe closely multiplication operation involves two steps one is producing partial products and adding these partial products [15]. Thus, the speed of a multiplier hardly depends on how fast generate the partial products and how fast we can add them together. If the number of partial products to be generated are of less than it is indirectly means that we have achieved the speed in generating partial products. Booth's algorithms are meant for this only. To speed up the addition among the partial products we need fast adder architectures. Multiplication consists of three steps: 1) Generate the partial products; 2) Add the generated partial products until the last two rows are remained; 3) Compute the final multiplication results by adding the last two rows. The modified Booth algorithm reduces the number of partial products by half in the first step.

We used the modified Booth encoding (MBE) scheme proposed. It is known as the most efficient Booth encoding and decoding scheme. Advanced multiplier capable of carrying out both signed and unsigned operations but suffers from complexity in generation of partial products [22]

Jipsa Antony, Jyotirmoy Pathak "Design of Baugh Woolley Multiplier using HPM Reduction Tree Technique" The main part of this paper is the reduction tree technique which is used for designing a new Baugh Woolley multiplier architecture. High Performance Multiplier (HPM) reduction tree [12] is based mainly on the generated partial product compression. It is completely regular and the connectivity of the adding cells in HPM is in the triangular shape. The reason for using triangular shaped is that the triangular cell placement in the reduction tree technique has a shorter wire length

The Baugh-Woolley multiplication is one of the efficient methods to handle the sign bots. This approach has been developed in order to design regular multipliers, suited for 2's complement numbers [18].

HPM Baugh Woolley multiplier is based on Hatamian's scheme [8]. It can be divided into three steps: 1) The most significant bit (MSB) of the partial-products in each N-1 rows and all bits of the last partial-product row, except its MSB, are inverted in the Baugh Woolley algorithm. 2) To the Nth column a '1' is added. 3) In the final result the MSB of it is inverted [12]. Implementation of Baugh Woolley multiplier using HPM method is simply a straight forward method, the partial products can be calculated using AND gates and the inverted products can be calculated using NAND gates. The disadvantages of this paper is it requires much area and become slow for higher number of operand bits and consumes more net power and internal power.

Himanshu Bansal, K. G. Sharma "Wallace Tree Multiplier Designs: A Performance Comparison Review", in this paper the Wallace multiplier [2] is an efficient parallel multiplier. In the conventional Wallace tree multiplier, the first step is to form partial product array (of N_2 bits). In the second step, groups of three adjacent rows each, is collected. Each group of three rows is reduced by using full adders and half adders. Full adders are used in each column where there are three bits whereas half adders are used in each column where there are two bits. Any single bit in a column is passed to the next stage in the same column without processing. This reduction procedure is repeated in each successive stage until

only two rows remain. In the final step, the remaining two rows are added using a carry propagating adder. The Wallace multiplier requires more half adder; need more number of gates so the area requirement is more. Wallace tree method offers high speed multiplication but circuit layout is difficult because of the structural irregularity [24].

Premananda B.S. et all, "Design and Implementation of 8-Bit Vedic Multiplier". The multiplier architecture is based on Urdhva Tiryagbhyam [3] (vertical and cross-wise algorithm) sutra. Illustration of Urdhva Tiryagbhyam sutra is shown in Figure 4.1.

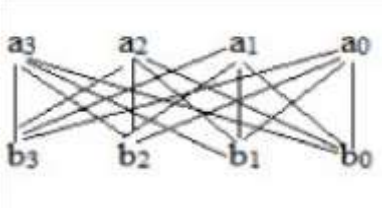

Figure 4.1. Illustration of Urdhva Tiryagbhyam sutra.

The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra [3], whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier. The 8-bit multiplier is designed using four 4x4 Vedic multipliers which employ Urdhva Tiryagbhyam sutra and carry skip technique for partial product addition. The output of these Vedic multipliers is added by modifying the logic levels of ripple carry adder.[26]. This method is the faster way compare to conventional multiplier, here in this method multiplication is carried out in Parallel. But the drawback of Urdhav-Triyakbhyam method is that if we consider the longer number it would become complex to calculate.

Pavan Kumar U.C.S, et all "FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter", This paper utilized 8-bit barrel shifter which requires only one clock cycle for 'n' number of shifts. The design is implemented and verified using FPGA and ISE Simulator. This paper put into effect a high speed Vedic multiplier using barrel shifter. The sutra was implemented by modified design of "Nikhilam Sutra" [3] due to its feature of reducing the number of partial products. The barrel shifter used at different levels of design drastically reduces the delay when compared to conventional multipliers. Assume that the multiplier is 'X' and multiplicand is 'Y'. Though the designation of the numbers is different but the architecture implemented is same to some extent for evaluating both the numbers. The mathematical expression for modified nikhilam sutra is given below.

$P=X*Y= (2^k2)*(X+Z2*2^(k1-k2))+Z1*Z2.$ – (1)

Where k1, k2 are the maximum power index of input numbers X and Y respectively. Z1 and Z2 are the residues in the numbers X and Y respectively.

The formula simply means: "all from 9 and the last from 10" The formula can be very effectively applied in multiplication of numbers, which are nearer to bases like 10, 100, 1000 i.e., to the powers of 10 . The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and only mental calculation. The numbers taken can be either less or more than the base considered.

Ex. 1: Suppose we want to multiply 9 by 7. Then:

Select as base for the calculation that power of 10 which is the nearest to the numbers to be multiplied (in our example 10 itself). Put the numbers to be multiplied, above and below on the left- hand as:

7

9

Subtract each from the base (in our example 10) and write down the remainders on the right-hand side as:

7 – 3

9 – 1

Between each of the numbers to be multiplied and the remainders put a connecting minus to show that the remainders are **less** than the base.

The result of the multiplication is a two digit number which will be written under the line. A vertical (/) dividing line may separate the left digit from the right digit of the product. The left-hand side digit can be obtained by cross subtract one deficiency in the second column from the original number in the left column. Both cross subtractions (i.e. 7-1 and 9-3) will give the same result:

7 – 3

9 – 1

6 /

The right-hand digit of the product is the result of the vertical multiplication of the remainders in the right column. 7 – 3

9 – 1

6 /3

Thus, the result is 63.

Now, if the numbers 98 and 97 must be multiplied, the base that has to be chosen is 100 and the Sutra (all from 9 and the last from 10) is used in order to perform on the spot the subtractions 100-98 and 100-97 and thus determine the numbers in the right column. In this example for the righthand side digit a two digit number must be obtained (since there are 2 zeros in our base not only one as before) Thus: 98 – 02

97 - 03
95 / 06

Thus, the result is 9506.

The disadvantages of Vedic multiplier using barrel shifter is consumption power In this design, efforts have been made to reduce the propagation delay and achieved an improvement in the reduction of delay[21].

Anuva Das et all "Design Optimization of Vedic Multiplier using Reversible Logic", in this paper presents Reversible logic is a new and promising field which addresses the problem of power dissipation. It has been shown to consume zero power theoretically. Vedic mathematics techniques have always proven to be fast and efficient for solving various problems. Therefore, in this paper we implement Urdva Tiryakbhayam algorithm using reversible logic thereby addressing two important issues – speed and power consumption of implementation of multipliers. Physical reversibility signifies a process that dissipates no energy to heat and logical reversibility states that earlier state of a process is ascertainable from the backward computation of a state at any given point of time. Complete physical reversibility is attainable only when the process is logically reversible [11]. Reversible implementation is done using a BVPPG gate, three Peres gates and a Feynman gate. This design needs five reversible logic gates, five constant inputs and generates five garbage outputs. Four 2x2 multipliers are arranged systematically. Each multiplier accepts four input bits; two bits from multiplicand and other two bits from multiplier. Addition of partial products are done using two four bit ripple carry adder, a two bit ripple carry adder and a half adder. We obtain the final result by concatenating the last two bits of the first multiplier, four sum bits of the second four bit ripple carry adder and the sum bits of two bit ripple carry adder. In two four bit and a five bit ripple carry adders are used to add the partial products of 2x2 block. But the block diagram suffers from a serious drawback due to the arrangement of adders [25]

V. CONCLUSION AND FUTURE WORK

In this paper, various multiplier with and without reversible have been discussed. A very good idea about various techniques used Vedic multiplier using reversible logic method is shown in this paper. As per study the above discussed papers are simple in terms of implementation but they lack in terms of low power. The negligible power can be achieved by Vedic multiplier based nikhilam sutra using Reversible logic. Speed is also a major factor. The techniques which are mainly affected by it are discussed in this paper.

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