Low Power SRAM design by Charge-Recycling assist Technique operating in Near Threshold voltage using 14nm Finfet Technology

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Abstract – This paper proposes a charge-recycling SRAM circuit design by using read and write assist scheme, the wasted charge in conventional read assist circuit can be efficiently recycled in write assist technique. The aim is to reduce the dynamic power consumption of SRAM assist technique using Near-Threshold voltage (NTV) operation in 14nm FinFET Technology. Although near-threshold voltage operation is an attractive means of achieving high energy efficiency, it can degrade the circuit stability of static random access memory (SRAM) cells. To reduce the Vth variations, fin-shaped field-effect transistors are used to reduce the random dopant fluctuation, which is a major contributor to Vth variations, using an undoped channel. Here, 7T SRAM cell consume low power when compared to other conventional 8T and 10T SRAM cell due to its single bitline structure. Thus the proposed SRAM circuit consume Less Power by operating it in NTV region.

Index terms — charge-recycling, low power design, Near-threshold voltage operation, SRAM cell, FinFET technology.

I.INTRODUCTION

As the demand for energy efficient portable and battery operated applications increases, low-power circuit designs are of fundamental importance. As the modern microprocessors and system-on-chips (SoCs) demand more and more embedded memories for system performance requirements, die area occupied by SRAM has been drastically increasing [1]. The trend motivates the efforts of SRAM designers to achieve a higher integration density as well as lower power consumption. With aggressive area scaling in nano-scale CMOS technology, the on-chip SRAM memories are becoming highly vulnerable to process variations, especially under low-voltage operation modes.

Recently, enhanced energy efficiency has been achieved by near- and sub-threshold digital circuit designs. In the sub-threshold region, energy efficiency can be maximized, but the performance is significantly degraded. The near-threshold region, in contrast, allows a balance between energy efficiency and performance. This tradeoff has led to circuit designers focusing on near-threshold voltage (NTV) circuit designs in mobile systems-on-a-chip (SoCs) [2]. SoCs with a supply voltage (*V*DD) reduced to NTV can achieve high energy efficiency with no significant degradation in performance.

However, the impact of variations in threshold voltage (*V*th) increase significantly in the NTV region, which endangers the stability of circuit operation. In particular, the increase in *V*th variations is critical to static random access memory (SRAM) cells, because these are typically designed using the minimum transistor size for high levels of integration. Thus, the read stability and write ability of SRAM cells can be significantly degraded. This will limit the NTV operation. To reduce the *V*th variations, fin-shaped field-effect transistors (FinFETs) are widely

used in 14nm technology [7]. FinFETs reduce the random dopant fluctuation, which is a major contributor to *V*th variations, using an undoped channel. In addition, FinFETs can achieve better short-channel controllability owing to their thin body and 3D structure. Here the 7T SRAM cell with single bitline structure is used for both read and write operations which reduces the standby power.

In this paper, a novel charge-recycling SRAM assist circuit is proposed to reduce the dynamic power consumption of the assist techniques. In the proposed charge-recycling approach, by combining the read and write assist schemes, the wasted charge in conventional SBL technique can be efficiently recycled in NBL without incurring significant area overhead. The simulation results show the low power consumption of SRAM assist techniques and also presented to show the superiority of the proposed charge recycling SRAM assist technique.

This paper is organized as follows. Section II explains the existing 7T SRAM cell and its operation. Section III describes the proposed charge-recycling assist technique and its operation in near threshold voltage region. Section IV discuss about the simulation results and compared the energy, power and delay between nominal and near threshold voltage operation. Section V shows the conclusions.

II.EXISTING 7T SRAM CELL

A. Structure and Layout

Fig. 1 shows a schematic of the existing 7T SRAM cell. The SRAM cell consists of a cross-coupled inverter pair (PUL, PUR, PDL, and PDR), access transistor (PG), and transmission gate transistors (TP and TN). TP and TN are placed between the storage node (Q) and the input node of the right-side inverter (Q*'*). The BL and WWLB are column-based signals whereas WL and WWLA are row-based signals. The circuit can operated based on the input which is given to WL and BL. Fig.2 shows the layout of a single cell of the existing 7T SRAM cell. The 7T SRAM cell is 3%, 44%, and 36% smaller than the 8T, 10T, and 9T SRAM cells, respectively.

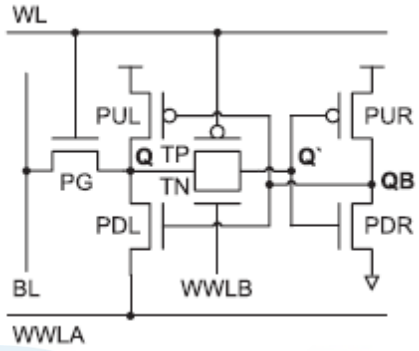

Fig.1. Schematic of the existing 7T SRAM cell.

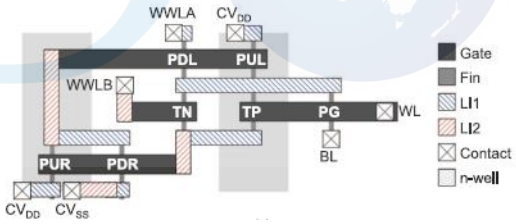

Fig.2. Single cell layout of existing 7T SRAM cell

B. Hold Operation in Active Mode

When the SRAM is in active mode but no read and write operations are performed, the SRAM cell is in hold mode. Fig. 3 shows the SRAM cell in hold mode, where only TP is turned on. If node Q stores high-state data, node Q*'* can maintain *V*DD, because the pMOS can pass a strong "1." If node Q stores low state data, the voltage at node Q*'* (*V*Q*'*) can rise above 0 V, depending on the sub-

threshold leakage current from node Q' to node Q and the gate leakage current from the right-side inverter. Because the gate leakage current is smaller than the sub-threshold leakage current due to a high-*k* process, the rise in *V*Q' is negligible. Thus, sufficient hold stability can be achieved, regardless of the stored data.

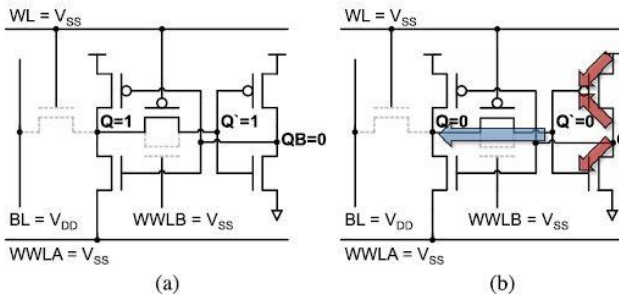

Fig.3. (a) Storing "1" data and (b) storing "0" data in hold mode.

C. Read Operation

Fig. 4 shows the read "1" and "0" operations in the existing 7T SRAM cell. During read operations, WL [3] in the selected row is forced to *V*DD and WWLA and WWLB are set to *V*SS. Thus, the transmission gate in the SRAM cell is turned off, which cuts the connection between nodes Q and Q'.

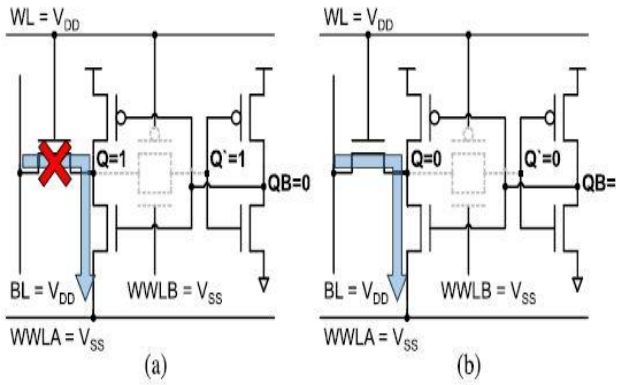

Fig.4. (a) Read "1" and (b) "0" operations of 7T SRAM cell.

After WL is enabled, the pre-charged BL is discharged to a low voltage level or maintained near *V*DD, depending on the stored data state. If node Q stores high-state data (read "1" operation), as shown in Fig. 4(a), the pre-charged BL is maintained near *V*DD. If node Q stores low-state data (read "0" operation), as shown in Fig. 4(b), the voltage at node Q (*V*Q) increases because of the voltage-dividing effect between the PG and PDL transistors. In the conventional 6T SRAM cell, if *V*Q increases above *V*trip in the right-side inverter, the stored data in the SRAM cell is flipped. In the 7T SRAM cell, the increased *V*Q does not affect the right-side inverter, because the input of the right-side inverter is decoupled (node Q') from node Q by the transmission gate. Although node Q' is decoupled from node Q, it can be increased by the gate leakage current from the right side inverter and the capacitive coupling effect between WL and node Q' when WL is enabled, because node Q' is floating, as shown in Fig. 4(b).

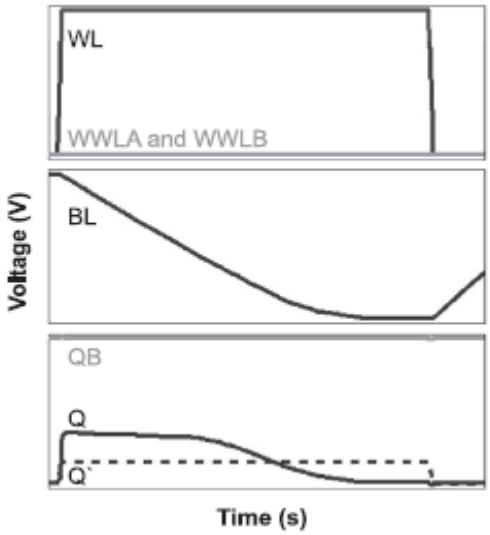

Fig. 5. Waveforms of the read operation in the existing 7T SRAM cell.

D. Write Operation

Although the standby power consumption can be reduced by using a single BL structure, the writing "1" operation is difficult because the nMOS PG cannot pass a strong "1." The boosted WL voltage (*BV*WL) scheme can be used to improve the write ability [3], but cannot sufficiently improve the writing "1" margin. Instead, the reduced *CV*DD below *V*DD [4] or the virtual floating source of the PD can be used. However, these solutions incur a large power overhead compared with the *BV*WL scheme, because the control signal of all selected columns must be controlled. In addition, both solutions degrade the hold stability of the column half-selected cells (CHSCs), which are the unselected cells in the selected column, because the difference between *CV*DD and *CV*SS becomes small. Thus, these techniques are not suitable for NTV

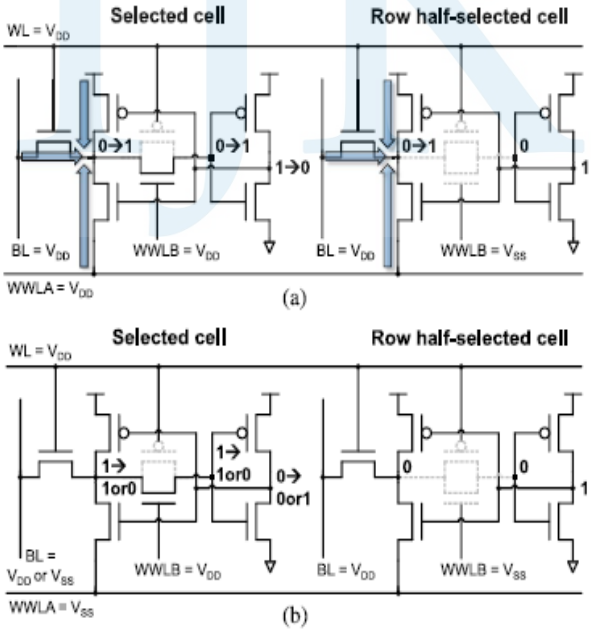

Fig.6. (a) Phase 1 and (b) phase 2 of the write operation of 7T SRAM cell.

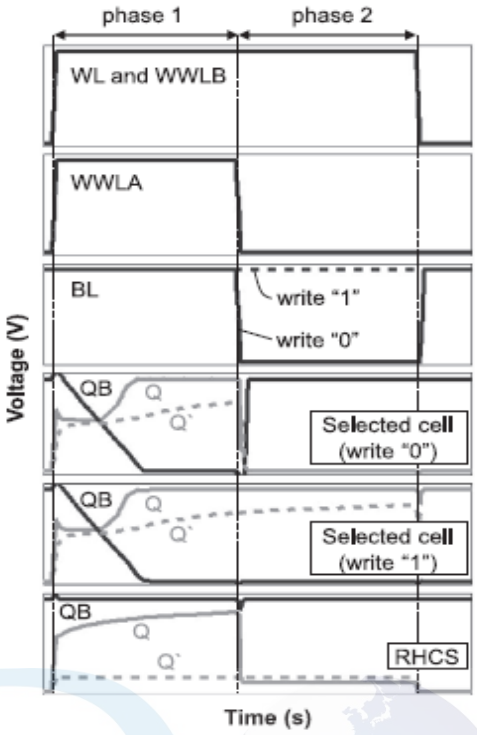

Fig.7. Waveforms of the write operation of the existing 7T SRAM cell.

operation. To resolve the previous write assist circuit for the writing "1" operation, the 7T SRAM cell employs a two-phase write operation, as shown in Fig.6. The two-phase approach the operation can be performed for both selected and half-selected cell in both the phases. In phase 1, high-state data are written to all selected SRAM cells without any problems, regardless of the state of the input data, as shown in Fig. 6(a). In phase 2, low-state data are selectively written to SRAM cells, as shown in Fig. 6(b).

III. PROPOSED CHARGE RECYCLING ASSIST TECHNIQUE

A. Charge-Recycling SRAM Assist Technique

Fig.8. shows the schematic and timing diagram of the proposed charge-recycling SRAM assist technique.

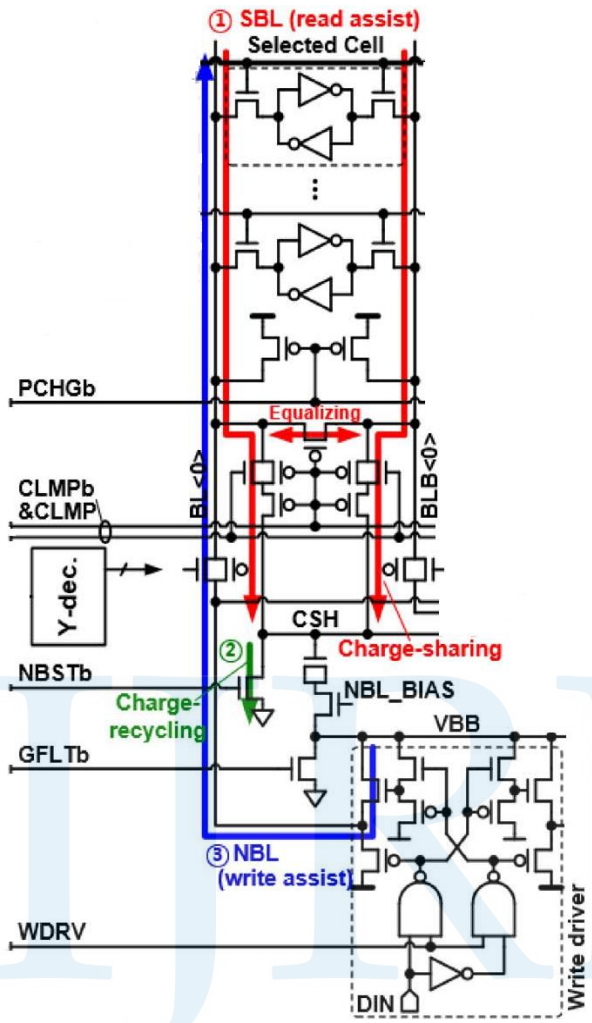

Fig.8. Schematic of proposed charge-recycling assist technique

The main idea is that the stored charge on the pre-charged BL, which has been dissipated directly in the conventional SBL, which can be re-used for the NBL technique to reduce the assist power consumption in the circuit. As shown in Fig. 8, in addition with conventional column peripheral circuits (precharge circuit, column-interleaving mux and write driver), the charge-sharing capacitor and BL clamper are added in the proposed charge-recycling SRAM assist circuit.

The detailed operation is explained as follows. Before the write and read operation, the charge sharing node (CSH) between the BL clamper and charge-sharing capacitor is pre-discharged to 0 V (*V*SS) and the BL pairs are pre-charged to *V*DD. When the write or read operation starts, the BL clampers are activated by the clamper enable (CLMP) signal. Then, the stored charge in the BL pairs flows through the charge-sharing capacitors (initially *V*SS) until the voltage levels of BL pairs and CSH node become equal. Based on the capacitance ratio between the BL pairs and CSH node, this suppressed BL voltage level can be determined. For the write assist technique, the negative voltage is generated by recycling the stored charge in the CSH node. After the sharing of charges in the BL clamper, the write-driver enable signal (WDRV) is asserted for the write operation. At this time, as shown in Fig. 8, the positive edge of the CLMPb signal increases the CSH node voltage.

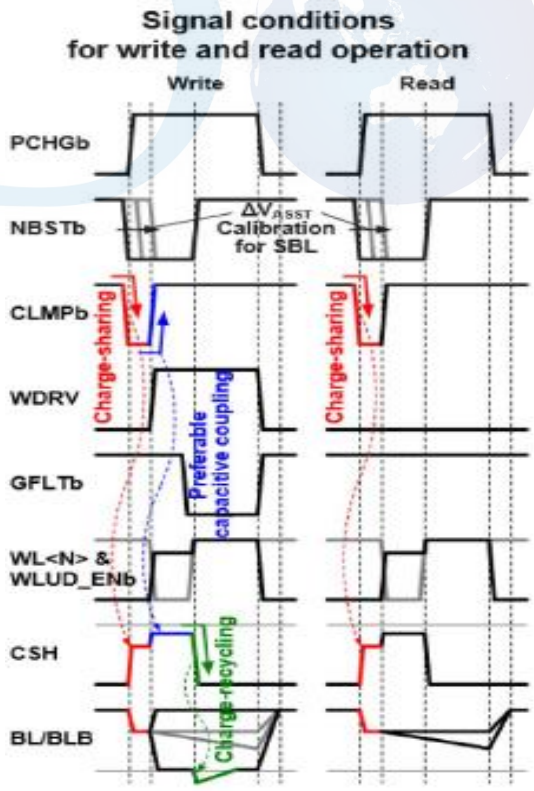

Fig.9. Timing diagram of proposed charge-recycling assist technique

Due to the opposite polarity between the CLMP and CLMPb signals, the pass-gates that are directly connected to BLs, reduces the impact of the capacitive coupling on the BLs. When the BLs are biased to the written data, the ground floating signal (GFLTb) is enabled to make the CSH node as floating state. At the same time, the falling edge of the CSH node is controlled by the negative boost (NBSTb) signal, which generates a negative voltage in the virtual ground (VBB) node. This charge-recycling scheme can effectively reduce the dynamic power consumption of the proposed assist technique by operating in near-threshold voltage region. Fig.9. shows the timing diagram of the proposed charge-recycling assist technique.

Hence, the above circuit can be operated in Near-Threshold voltage operation to show the reduction in power consumption of SRAM circuit. Although near-threshold voltage operation is an attractive means of achieving high energy efficiency, it can degrade the circuit stability of static random access memory (SRAM) cells. To reduce the Vth variations, fin-shaped field-effect transistors (FinFET) are used to reduce the random dopant fluctuation, which is a major contributor to Vth variations, using an undoped channel.

B. Near-Threshold computing

The modern CMOS circuits results in charging and discharging of internal node capacitances and which can be reduced quadraticallycby lowering supply voltage (Vdd). As such, voltage scaling is more effective method to reduce power consumption in commercial parts. It is well known that CMOS circuits functions at very low voltages and remain functional even when Vdd drops below the threshold voltage (Vth). In 1972, Meindl et al. derived a theoretical lower limit on Vdd for functional operation, which has been approached in very simple test circuits. Since, the interest in sub-threshold operation for analog circuits are recently more for digital processors, denoting operation at Vdd below 200 mV. However, the lower bound on Vdd in commercial applications is typically set to ~70% of the nominal Vdd due to concerns about robustness and performance loss. Given this wide voltage scaling potential, it's important to determine the Vdd at which the energy per operation is optimal. In the super threshold region (Vdd > Vth), energy is highly sensitive to Vdd due to the quadratic scaling of switching energy with Vdd. Hence down scaling to the near-threshold region (Vdd~ Vth) [8] yields an energy reduction on the order of 10X at the expense of approximately 10X performance degradation, as seen in Fig.10. However, the dependence of energy on Vdd becomes more complex as voltage is scaled below Vth. In sub-threshold (Vdd < Vth), circuit delay increases exponentially with Vdd, causing leakage energy (the product of leakage current, Vdd, and delay) to increase in near-exponential manner. This rise in leakage energy eventually dominates any reduction in switching energy, creating minimum energy consumption as shown in Fig. 10. The identification of an energy minimum which led to interest in processors that operate at this energy optimal supply voltage (referred to as Vmin and typically 250 mV–350 mV). However, the energy minimum is relatively shallow. Energy typically reduces by only ~2X when Vdd is scaled from the near-threshold region (400–500 mV) to the sub-threshold region, though delay rises by 50–100X over the same region. In ultra low energy sensor-based systems, this delay penalty is not tolerable for a broader set of applications. Hence, although introduced roughly 30 years ago, ultra low-voltage design remains confined to a small set of markets with little or no impact on mainstream semiconductor products.

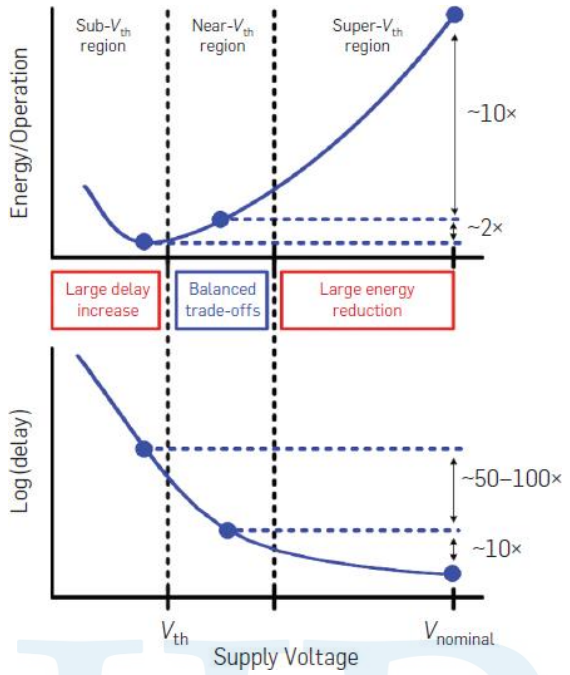

Fig.10. Energy and delay in different supply voltage operating regions.

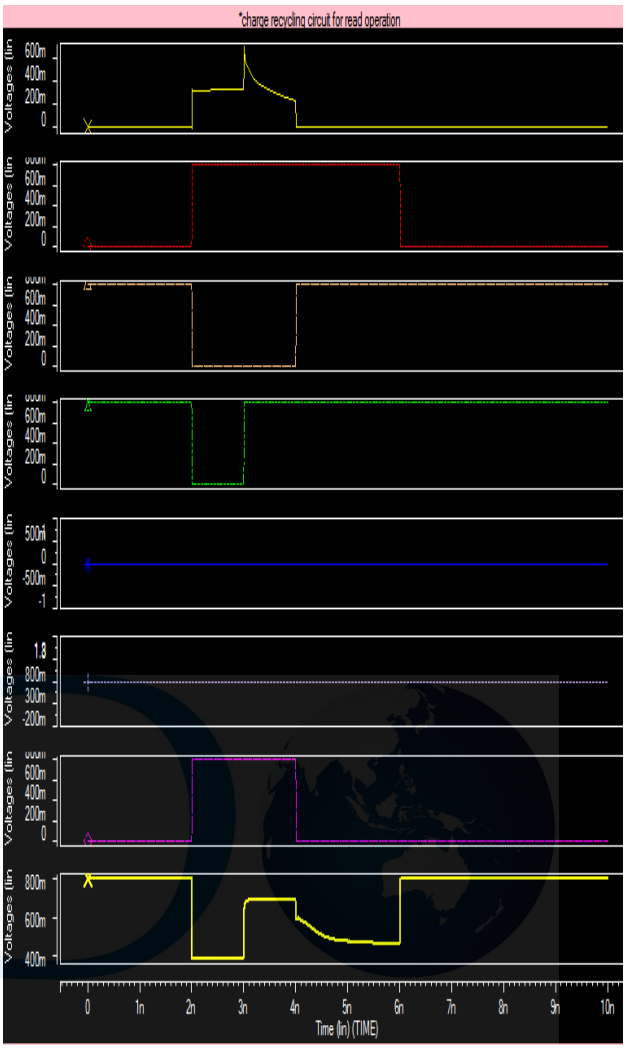

Fig.11. Read operation in charge-recycling assist technique in nominal voltage mode a).CSH, b).PCHGb, c).NBSTb, d).CLMPb, e).WDRV, f).GFLTb, g).WL, h).BL

IV. SIMULATION RESULTS AND COMPARISON

A. SIMULATION RESULTS

In this section, the proposed charge-recycling assist technique which is operated in nominal and near-threshold voltage are compared and simulated as shown below in the following figures.

The above graph shows the read operation in nominal voltage region. By applying a voltage of 0.8v the operation can be perfomed. a). CSH, denotes a charge sharing node in which a charge can be shared between the bit-line clamper and the charge sharing capacitor. b). PCHGb, denotes a precharge signal, before going for a operation the bit-line can be pre-charged.
c). NBSTb, denotes a negative booster which is used for the connection with a ground-return system to reduce the potential

difference between the two points on the ground return path. d).CLMPb, tells about a clamper enable signal which maintain the voltage limits of a signal at prescribed levels. e). wdrv, shows the write driver signal which is an electrical circuit used to control the other circuit components. f).GFLTb, explains about the ground floating signal, when the ground is said to be floating when the connection does not exist. g). wl is word-line which is used to read the data in row direction. h). BL is used to read the data in column direction.

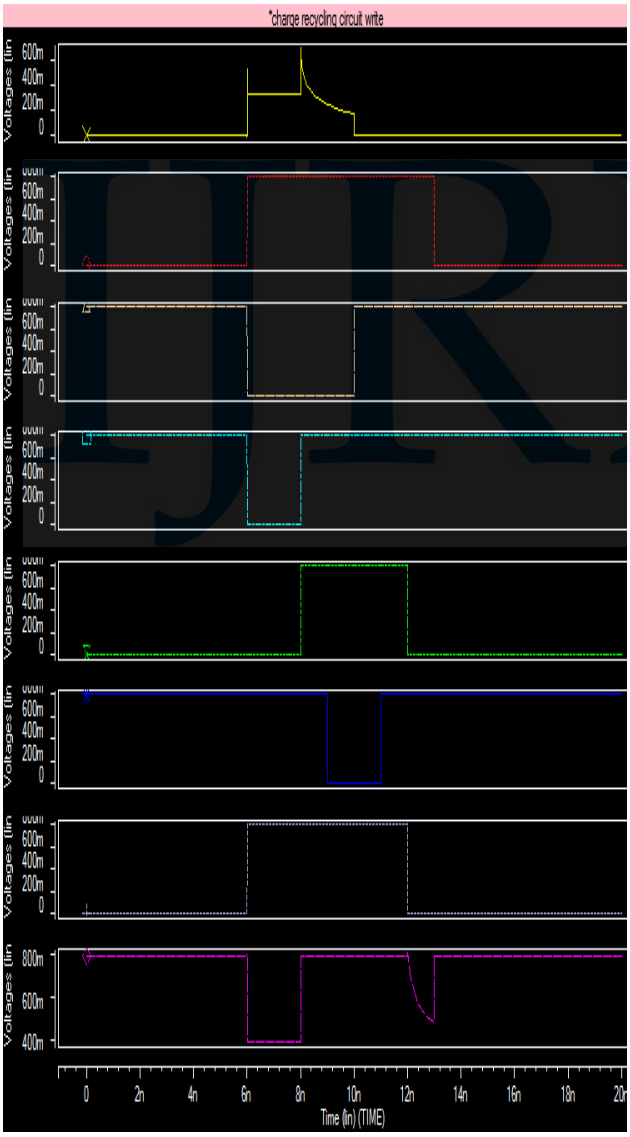

Fig.12. Write operation in charge-recycling assist technique in nominal voltage mode a).CSH, b).PCHGb, c).NBSTb, d).CLMPb, e).WDRV, f).GFLTb, g).WL, h).

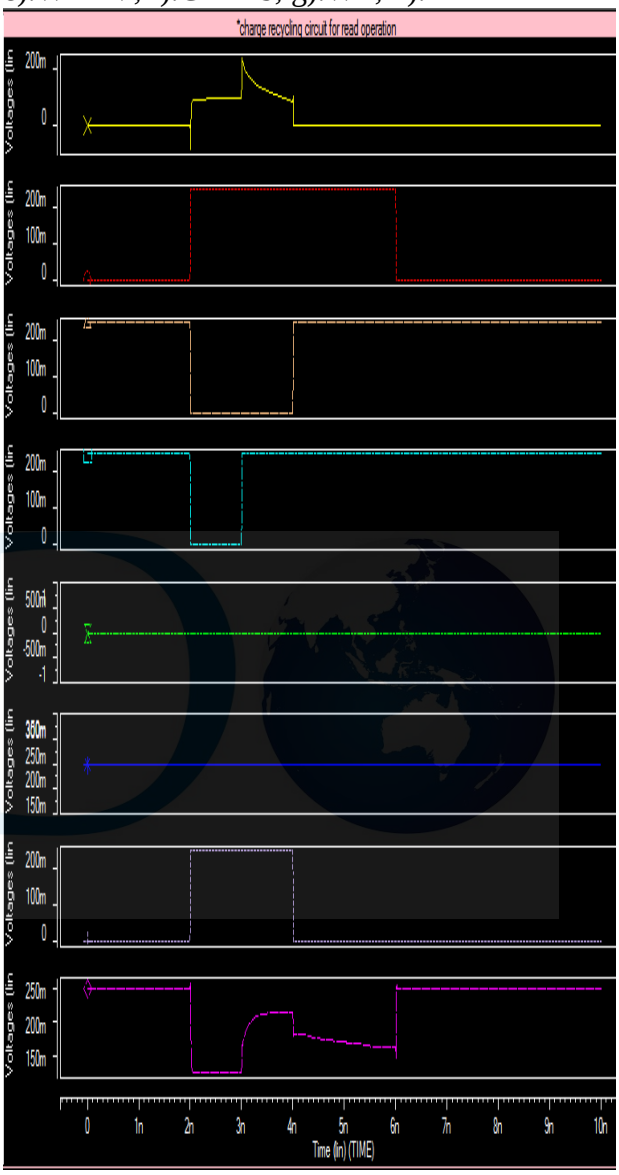

Fig.13. Read operation in charge-recycling assist technique in NTV mode a).CSH, b).PCHGb, c).NBSTb, d).CLMPb, e).WDRV, f).GFLTb, g).WL, h).BL

The above figure shows the read and write operation in NTV region. By applying a voltage of 0.25v, the operation can be performed by giving various inputs signal. Here, the power consumption is very much

reduced in Near-threshold region. The main aim of NTV is to achieve the energy efficiency by consuming low power. In comparison with nominal voltage, the power consumption is very much reduced in Near-threshold region.

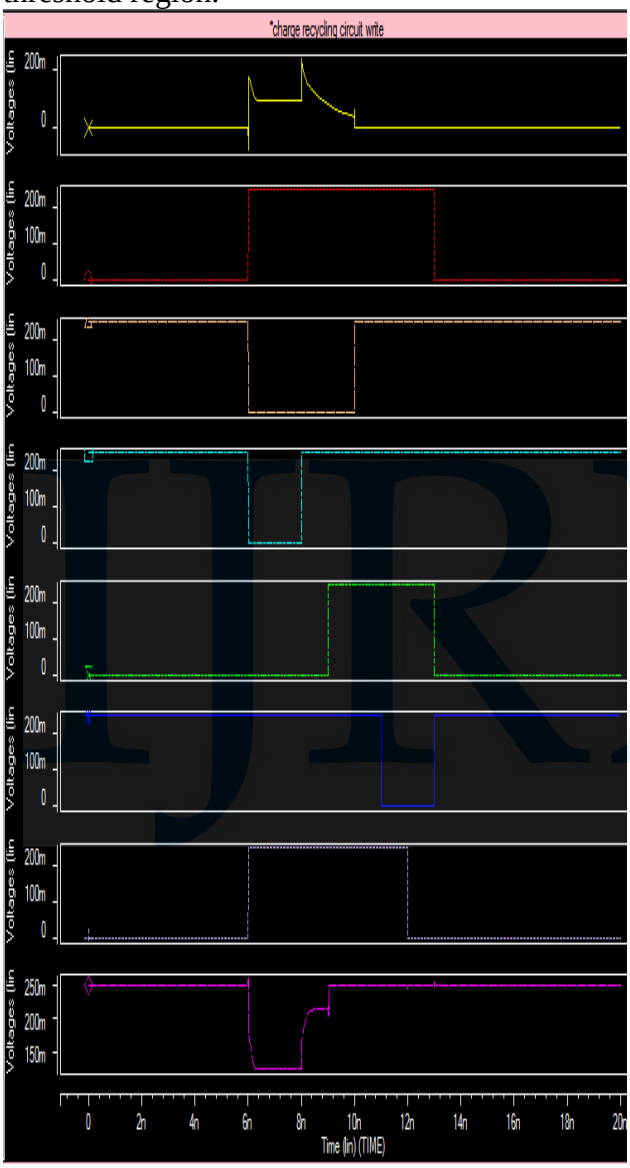

Fig.14. Write operation in charge-recycling assist technique in NTV mode a).CSH, b).PCHGb, c).NBSTb, d).CLMPb, e).WDRV, f).GFLTb, g).WL, h).BL

B. COMPARISON TABLE

The above Fig.5.1 shows the difference between energy, power and delay between nominal and near-threshold voltage. From this, the power and energy for near-threshold voltage is low when compared to the nominal voltage but the delay in NTV is high when compared to nominal voltage. This shows that when the device power reduces then it increases the delay.

Para-meter	Read op. in nom. voltage	Read op. in NTV	Write op. in nom. voltage	Write op. in NTV
Energy	36.3958 (fJ)	1.7637 (fJ)	78.0852 (fJ)	3.7648 (fJ)
Power	3639.6 (nW)	55.1165 (nW)	3904.3 (nW)	58.8251 (nW)
Delay	998.0437 (ps)	2.6198 (ps)	1997.8 (ps)	1.9211 (ps)

CONCLUSION

In this work, to reduce the dynamic power consumption of the SRAM cell, a novel charge-recycling SRAM assist technique is presented. By combining the read and write assist schemes, the wasted charge in conventional read assist circuit can be efficiently recycled in write assist technique. Near-threshold voltage operation is meant for energy efficiency application. By operating the circuit in near-threshold voltage operation, energy efficiency can be achieved and the power consumption of the SRAM cell

is reduced by using 14nm FinFET technology. And the power, energy and delay comparison were made for the nominal and near-threshold voltage. The power consumption in NTV operation is less in comparison with nominal voltage operation.

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