Cascaded H-Bridge Multilevel Inverter with Unequal DC Sources

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***Abstract* – Now a days the development of enthusiasm for multilevel inverters has been expanding on the grounds that there are huge uses of there in FACTS and modern drives and so on., Although there are numerous topologies of multilevel inverters in literature, mainstream among them are cascaded H-bridge. All in all the control techniques for these cascaded inverters are planned a suspicion of having all dc source voltages same for all H-bridges. This paper examines the capacities of cascaded multilevel inverter to create more output voltage levels with same number of H-bridges, yet with various input voltage proportions. The ideal nature of input dc voltage sources is shown as advantage in this paper. Total Harmonic Distortion (THD) is analyzed by simulation in MATLAB / Simulink.**

Keywords- multilevel inverters; cascaded H-bridge; Total Harmonic Distortion.

I. INTRODUCTION

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Inverters can be broadly classified into single level inverter and multilevel inverter. Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and can operate on several voltage levels. A multi-stage inverter is being utilized for multipurpose applications, such as active power filters, static var compensators and machine drives for sinusoidal and trapezoidal current applications. The drawbacks are the isolated power supplies required for each one of the stages of the multi converter and it's also lot harder to build, more expensive, harder to control in software.

Major electric drives and utility applications require advanced power electronics converter to meet the powerful requirements. Therefore, multilevel power converter structure has been presented as an option in high power and medium voltage circumstances. A multilevel converter accomplishes high power appraisals, as well as enhances the execution of the entire system as far as harmonics, dv/dt burdens, and stresses in the bearings of the motor.

A few multilevel converter topologies have been produced; i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature surveys, the cascaded multilevel inverter (CMI) with isolated DC sources is unmistakably the most possible topology for use as a power converter for medium and high power applications because of their modularization and extensibility. The H-bridge inverter disposes of the unreasonably expansive number of (i) massive transformers required by routine multilevel inverters, (ii) clamping diodes required by multilevel diode - clamped inverters, , and (iii) flying capacitors required by multilevel flying-capacitor inverter.

In this paper, simulation work is carried out on 1-φ and 3-φ 7-level, 19- level and the 25-level cascaded H-Bridge multilevel inverter and THD analysis is carried out. With the introduction of unequal DC levels different output voltage levels can be obtained in a single circuit. The proposed topology will generate along with the zero level, equal number of negative levels and positive levels. However by the series connection of the proposed basic units it is possible to generate 19-level output voltage levels i.e 9-level in positive,9-level in negative and zero level.it is also possible to generate 21-level output with the same topology i.e 10-level in positive and 10-level in negative and zero level. Same can be applied to 25 level too.

II. MULTILEVEL INVERTERS

These inverters make a stepped voltage waveform by method for various dc voltage sources as the input and a reasonable plan of the power semiconductor-based devices. Three significant structures of the multilevel inverters have been introduced: "diode clamped multilevel inverter," "flying capacitor multilevel inverter," and "cascaded multilevel inverter". The cascaded multilevel inverter is gathered of various single-stage H-bridge inverters and is classified into symmetric and asymmetric groups in light of the extent of the magnitude of dc voltage sources. In the symmetric sorts, all the dc voltage sources of cascaded H-Bridges are

having equal magnitudes, though in the asymmetric sorts, the values of the dc voltage sources of all H- bridges are unique. In topical years, various topologies with different

In and, assorted symmetric cascaded multilevel inverters have been exhibited. The first point of interest of all these structures is the short variety of dc voltage sources, which is a standout amongst the most noteworthy elements in deciding the expense of the inverter. Then again, on the grounds that some of them use an elevated number of bidirectional power switches, a high number of integrated gate bipolar transistors (IGBTs) are vital, which is the major downside of these topologies. Therefore, it expands control complexity nature, circuit size and cost. The significant point of interest of this asymmetrical topology and its algorithms is related to its capacity to make a considerable number of output voltage levels by utilizing a low number of dc voltage sources and power switches however the high assorted qualities in the extent of dc voltage sources is their most extraordinary disadvantage.

As of late, asymmetrical and hybrid multilevel topologies are getting to be a standout amongst the most interested exploration territory. In the deviated designs, the magnitudes of dc voltage supplies are uneven. These topologies decrease the expense and sizes of the inverter and show signs of improvement dependability since lesser number of power electronic parts, capacitors, and dc supplies are utilized. The hybrid multistage converters comprise of divergent multilevel setups with uneven dc voltage supplies. Bidirectional switches with a reasonable control system can upgrade the execution of multilevel inverters as far as falling the quantity of semiconductor segments, minimizing the withstanding voltage and accomplishing the required output voltage with more elevated amounts. The extents of the used dc voltage supplies have been chosen in a way that brings the lifted number of voltage levels with an effective application of a fundamental frequency staircase modulation technique.

For a 1-φ seven-level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Uneven voltage innovation is utilized as a part of the cascaded H-bridge multilevel inverter to permit more levels of output voltage, so the cascaded H-bridge multilevel inverter is appropriate for applications with expanded voltage levels. Two H- bridge inverters with a dc voltage of numerous connections can be associated in cascaded to create a single stage seven-level inverter and eight power electronic switches are utilized. In this paper another asymmetrical Bi-directional converter topology which utilizes conflicting proportions of dc voltage sources is implemented.

control systems have been introduced for cascaded multilevel inverters

III. PROPOSED CONCEPT

Hybrid Multilevel Inverter was presented by method for all 3M conceivable output voltages, where M is the quantity of modules allied in series arrangement. In spite of the fact that this inverter utilizes to a great degree diverse DC voltage sources in the connection of 1:3:9 and so on. In recognize, the DC voltage sources consider in this paper are still astoundingly near each other, they vacillate just by ±20 %. The amount of cells in grouping decides the quantity of output levels. 3M= 27 switching states, when M= 3 cells. With comparable DC voltages, there are various switching states that make the same output voltages, bringing about 2.M + 1 = 7 distinctive stage output voltage levels. Uneven DC source voltages direct to an enhanced number of various output voltage levels. The most extreme number of levels is 3M = 27. With the DC source voltages dispersed as Viii :Vi12 : Vil3 = 1Voc : 3Voc : 9Voc, all the divergent output voltage levels are reliably separated. The point of such an inverter (Hybrid Multilevel Inverter) has the weakness that the preliminary modularity is vanished. Every module must be proposed for the proportional voltage class.

At the point when the DC source voltages are uneven however just ±20 % not at all like from each other, the quantity of various OUTPUT voltage levels is likewise prevalent. As a case, we trust a situation where one cell has 100 % of its nominal DC voltage, other has 120% and the third one has 80%. The DC source voltages are in connection of 4:5:6 in this plan. As can be seen, the voltage levels are around the same as in the 1:3:9 case, aside from some levels not there at high complete estimations of output voltage.

The below figure shows the output wave forms the proposed asymmetrical converter. It is clearly seen that the level of inverter varies with the change in the ratios of input voltage. The inverter gives 21 level output voltage when the ratio is 1: 2: 7, while it gives 19 level output voltage when the ratio is 1:2:6 and it gives 25 level output voltage when the ratio is 1:3:8. This inverter having 3 bridges connected in series gives different levels of output voltages without changing the circuit except the ratios of input voltages. Switching of the converter is done by following the staircase control technique. Pulse width Modulation technique can also be applied by appropriate calculation of the switching time period

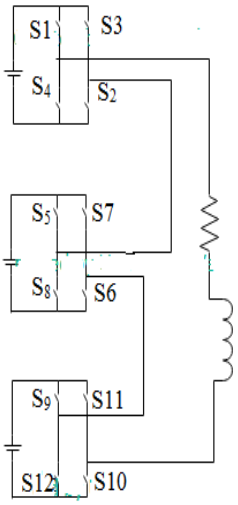

Fig.1 19-level with ratio 1:2:6

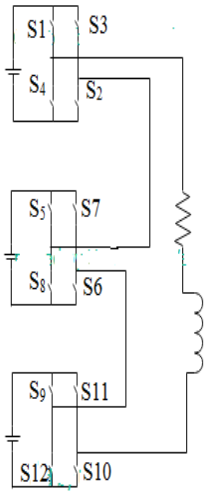

Fig 2. 21-level with ratio 1:2:7

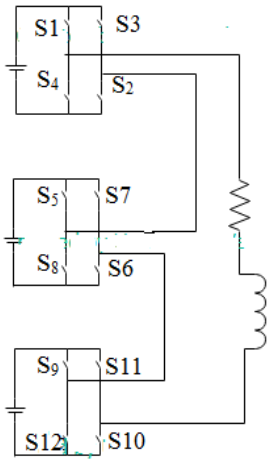

Fig.3 25-level with ratio 1:3:8

IV. HARDWARE

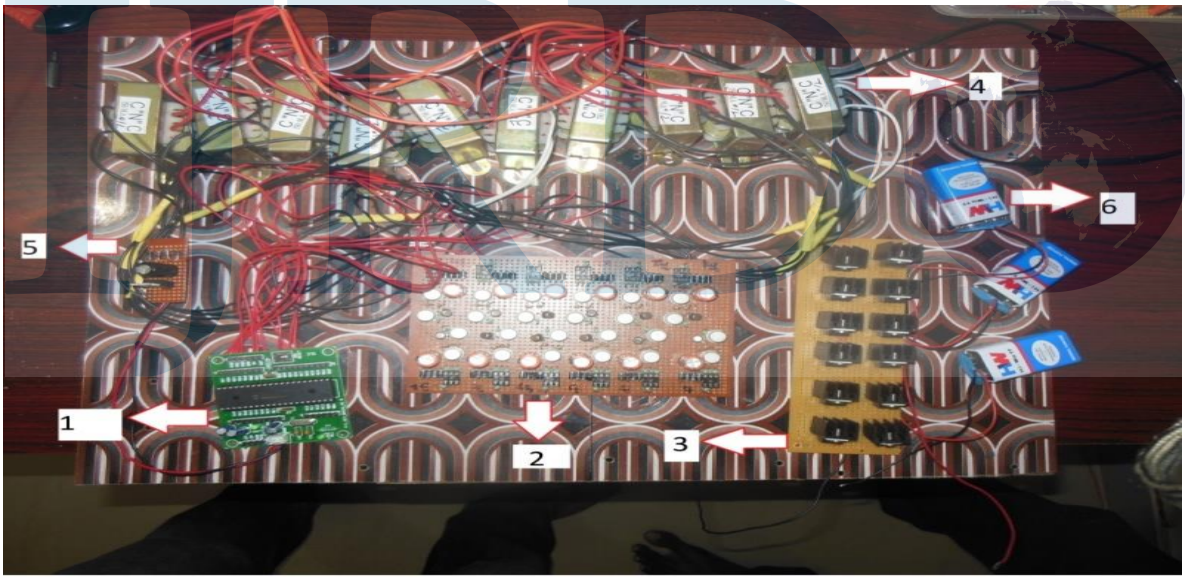

Fig.4. Hardware Unit

The hardware is as shown above. It consists of the below mentioned parts

A. Controller: Oscillator in the controller unit is mainly responsible for maintaining the oscillating frequency. Its vale is 20 Mhz. Programme is dumped in the PIC microcontroller IC. 12 output pulses for the driver circuit of 0-5V is supplied by the controller. The input to the controller is given by the rectifier unit. Input is applied between the 5V and ground.

The output pins are from RB_0 to RB_7 of "B" Port and from RD_4 to RD_7 of "D" port.

B. Driver Unit: Driver unit provides the isolation for the control circuit and for other High voltage circuits. The isolation is provided by the Octo-coupler

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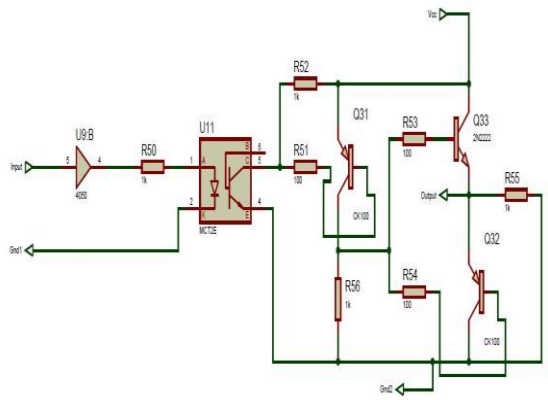

Fig.5 Driver Circuit

Input is given to 1K because buffer uses many number of pulses, say more than 20 and we have only 12 pulses to give it to the MOSFET's. The octo coupler MCT2E is very minimum i.e 7 to 8V and Current around 10mA. So we need to amplify the signal using one transistor. Transistor Q31 has input resistance of 100 ohm. Current to Q31 is calculated by

$$I=\frac{12}{100}$$

Output of Q31 is used to trigger Q32 and Q33.These two are trigger units. One is PNP and other is NPN. According to pulses, if it is zero it will be switching on PNP and it will apply diodes and the capacitor acts as a filter. 12 units of Driver units gate. It switches ON the MOSFET. For this amplification 12V DC is required and it is given by the bridge consisting of 4 supply pulses to 12 MOSFET0V to the gate and it switches OFF the MOSFET. If the pulse is high it will switch on the NPN which will apply 12V to the gate.

C. MOSFET(IRF540N) unit: This unit consists of the 12 MOSFETS. Unit of 4 comprises of a one inverter. Such 3 units are cascaded to give out the AC output voltage

D. Step Down Transformers: These transformers step down the AC 230V to the DC 12V. The output of the step down transformer is given to the rectifier unit. This rectifier unit rectifies the 12V DC to 5V dc supply to supply it to the input of the Controller.

E. Rectifier Unit: rectification is the conversion of alternating current (AC) to direct current (DC). This involves a device that only allows one-way flow of electrons. As we have seen, this is exactly what a semiconductor diode does. In our application we have used a full bridge rectifier circuit. A 5V regulator is used to maintain the constant output voltage for the PIC controller. Capacitor is used to provide the Action of filter

V. MATLAB SIMULATION

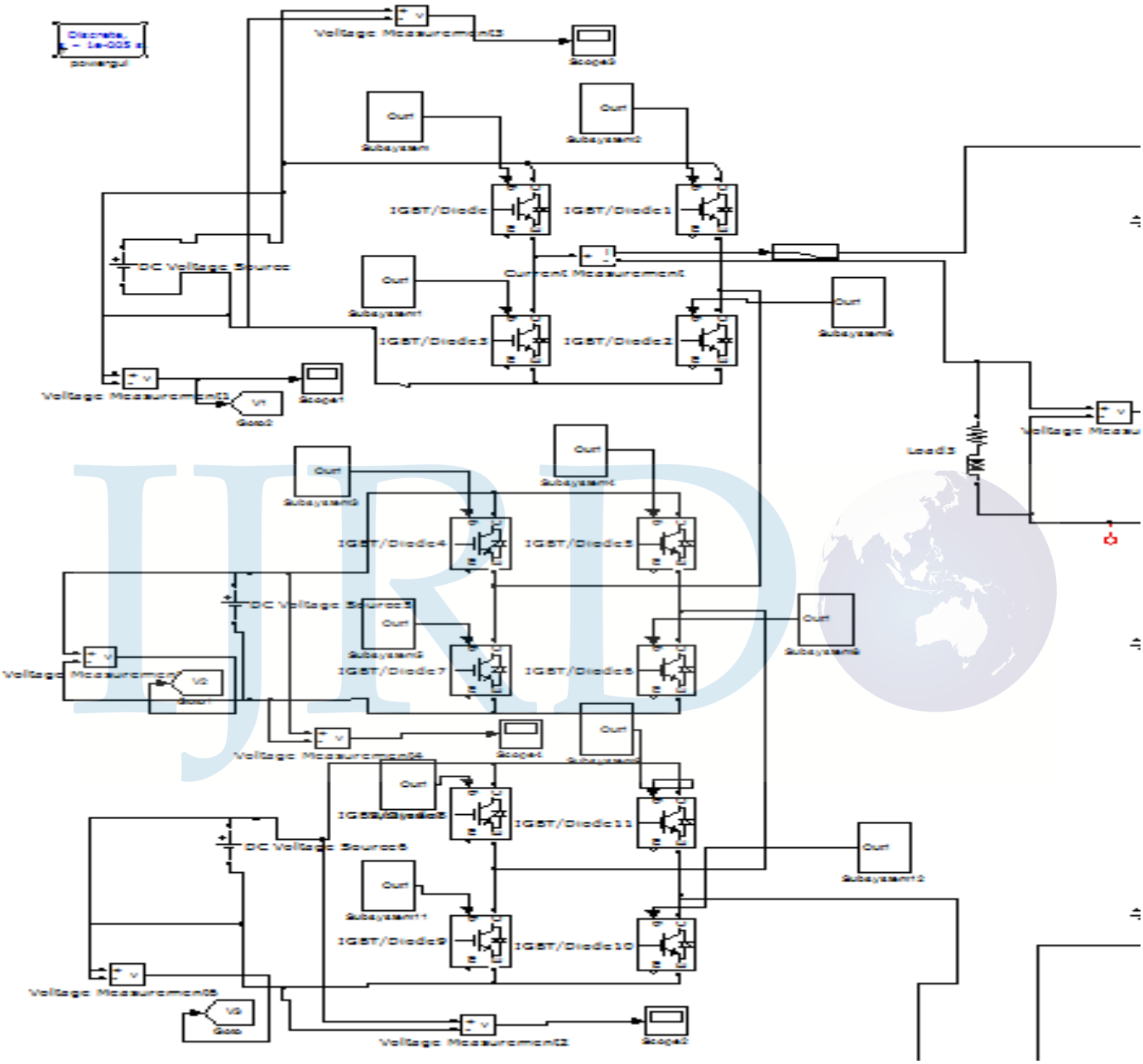

Fig.6. Matlab Simulation

The proposed concept is simulated by using the matlab simulink. The input provided is V1, V2, V3 of desired values in the appropriate ratios to get the output appropriate inverter levels. Power electronic switch used here is IGBT. The generated pulses by Staircase technique applied to the Gate of the IGBT. The pulses given to the gate are created inside a subsystem. An appropriate RL load is connected to the cascaded inverter. Above figure shows the 1-φ of the cascaded inverter. 3- φ can be simulated by providing the phase difference of 180 to all the 12 switches of the IGBT.

TABLE I

VOLTAGE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
O	O	O	O	O	O	O	O	O	O	O	O	O
V_1	1	1	O	O	O	1	O	D_8	O	1	O	D_{12}
V_2-V_1	O	O	D_3	D_4	1	1	O	O	O	1	O	D_{12}
V_2	O	1	O	D_4	1	1	O	O	O	1	O	D_{12}
V_2+ V_1	1	1	O	O	1	1	O	O	O	1	O	D_{12}
V_3- V_1- V_2	O	O	D_3	D_4	O	O	D_7	D_8	1	1	O	O
V_3- V_2	O	1	O	D_4	O	O	D_7	D_8	1	1	O	O
V_3- V_2+ V_1	1	1	O	O	O	O	D_7	D_8	1	1	O	O
V_3- V_1	O	O	D_3	D_4	O	1	O	D_8	1	1	O	O
V_3	O	1	O	D_4	O	1	O	D_8	1	1	O	O
V_3+ V_1	1	1	O	O	O	1	O	D_8	1	1	O	O
V_3+V_2- V_1	O	O	D_3	D_4	1	1	O	O	1	1	O	O
V_3+V_2	O	1	O	D_4	1	1	O	O	1	1	O	O
V_1+ V_2+ V_3	1	1	O	O	1	1	O	O	1	1	O	O

Switching Sequence

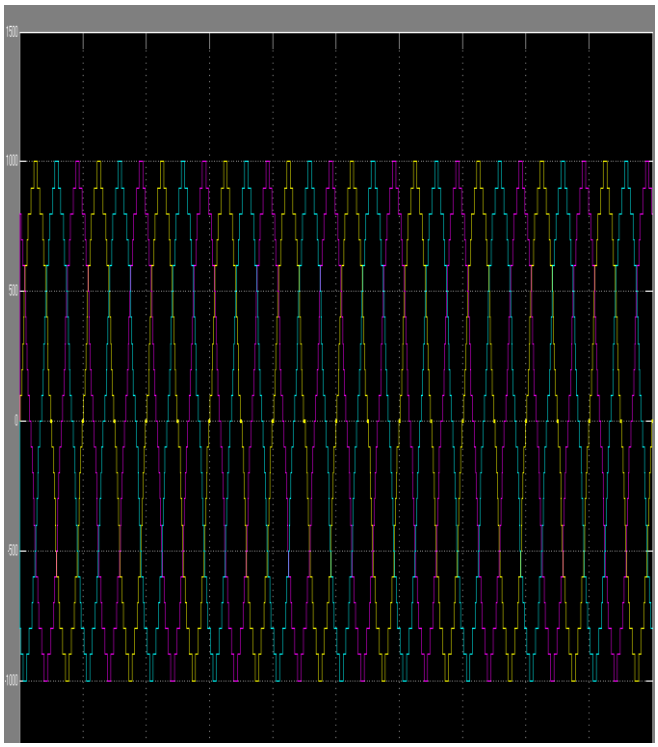

Fig.7. 21-Level voltage waveform

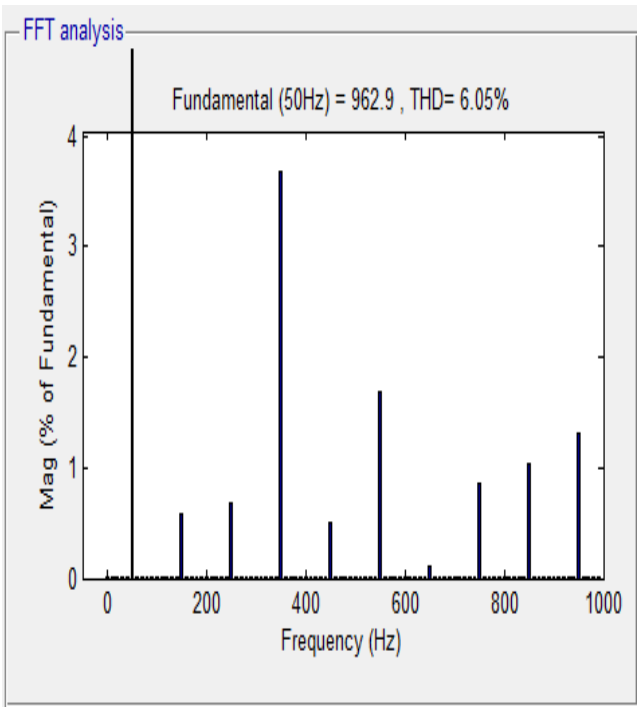

Fig.9. 7-level Voltage THD

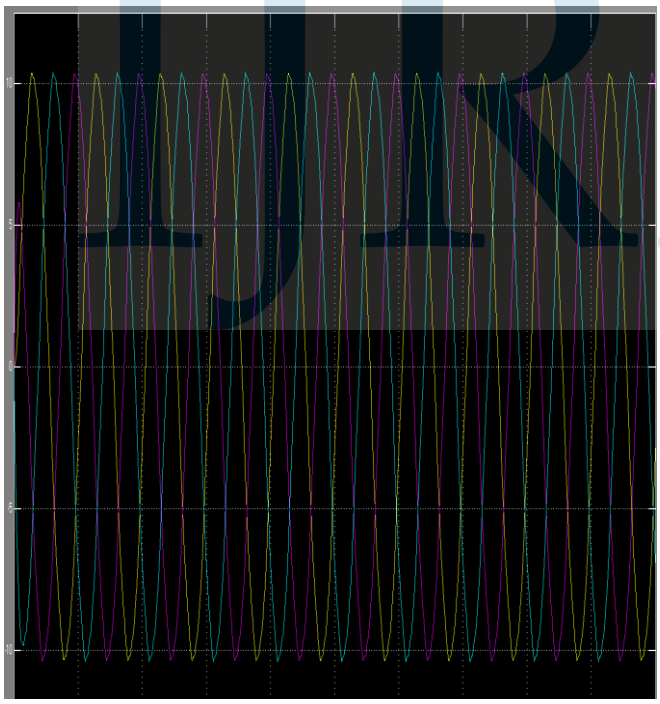

Fig.8 21-Level current waveform

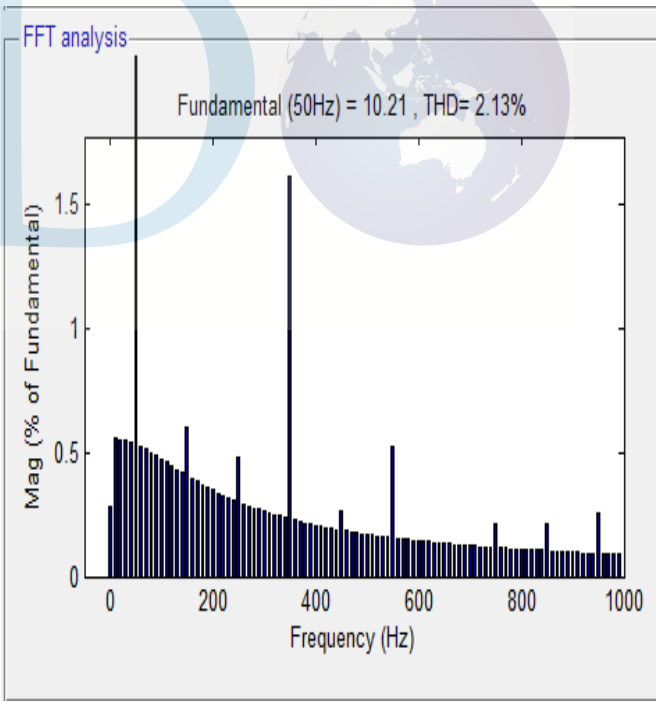

Fig.10. 21-Level current THD

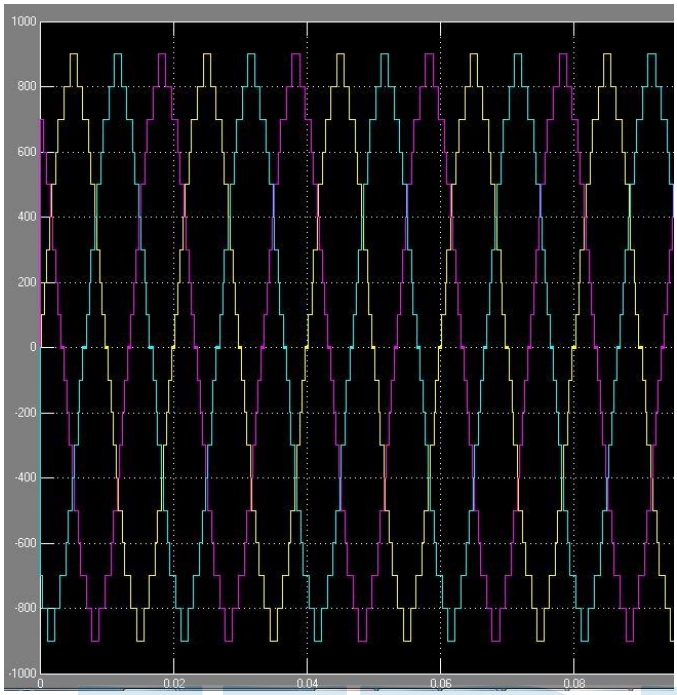

Fig.11. 19-Level voltage waveform

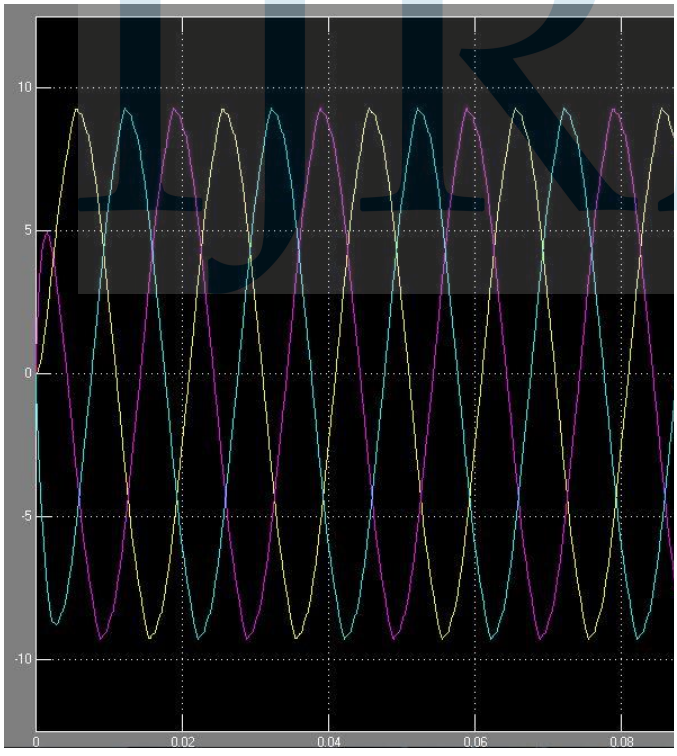

Fig.12. 19-Level current Waveform

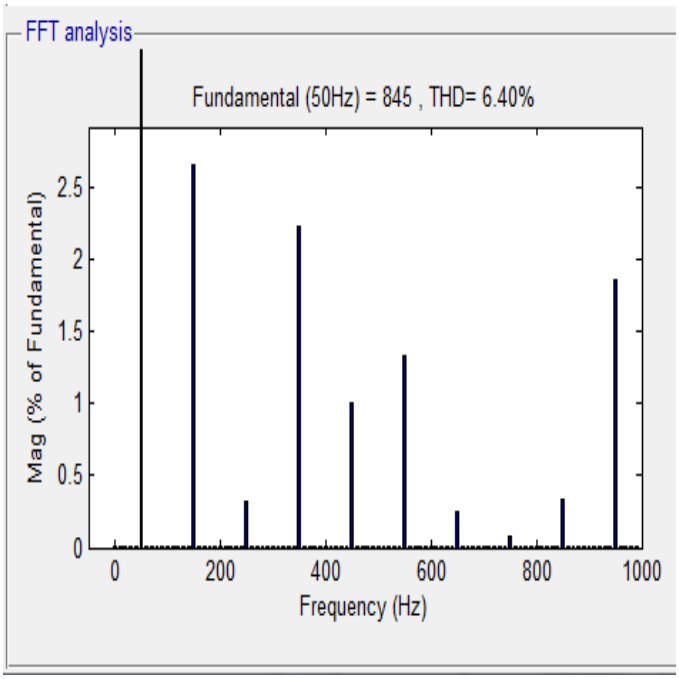

Fig.13. 19-Level Voltage THD

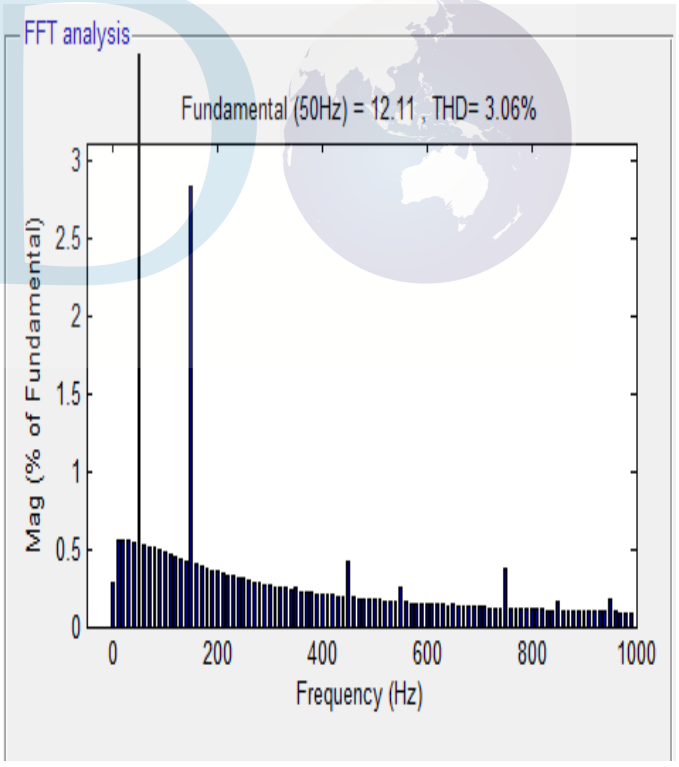

Fig.14.19-Level current THD

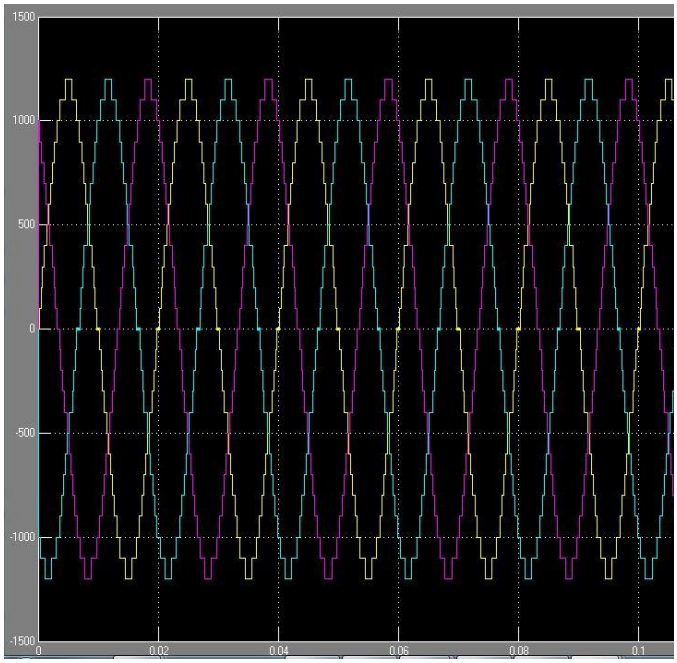

Fig.15. 25-Level Voltage waveform

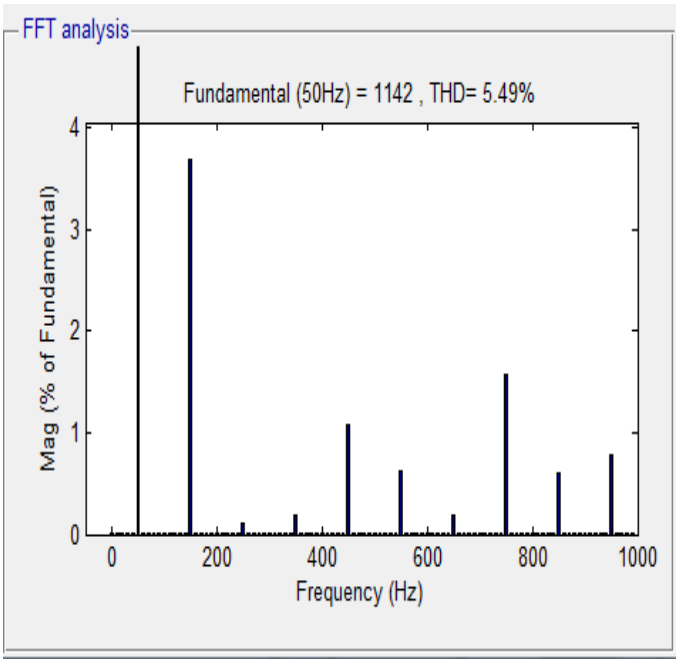

Fig.17. 25-Level voltage THD

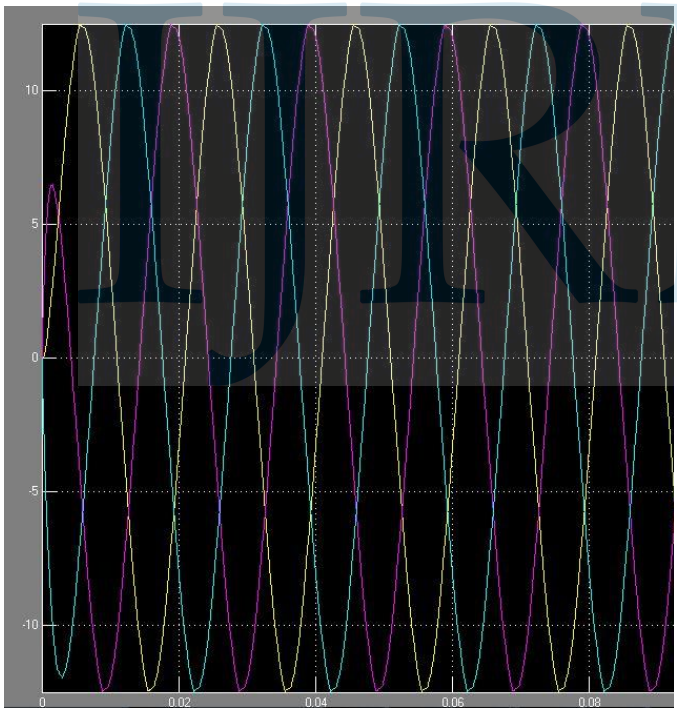

Fig.16. 25-Level current waveform

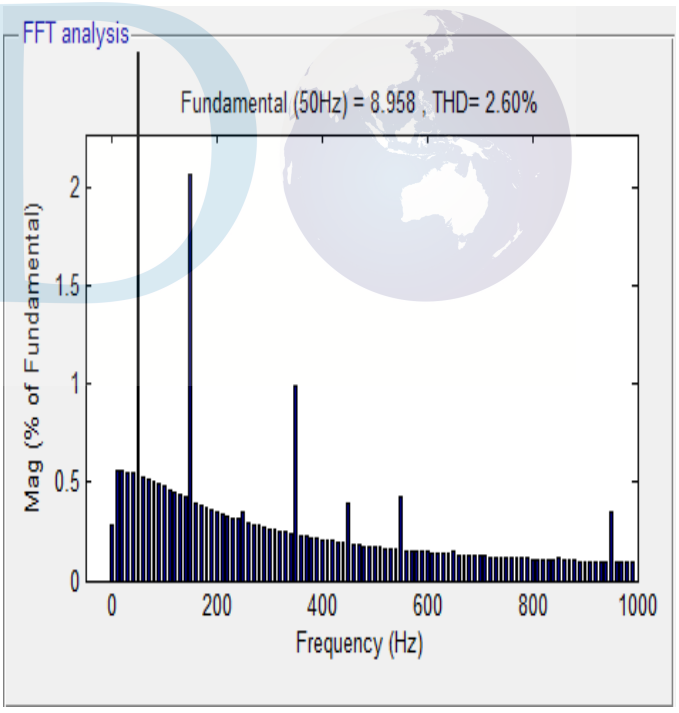

Fig.18. 25-Level current THD

VI. CONCLUSION

In this proposal the THD of the various multilevel outputs is analyzed. Simulation results show that the 3-Phase 7 level, 19 Level and the 25-Level Asymmetrical cascaded bridge are studied. Asymmetrical 7-Level cascaded H-bridge gives voltage THD of 13.40% where as the current gives 5.16%. Asymmetrical 19-Level cascaded H-bridge gives voltage THD of 6.40% where as the current gives 3.06%. Asymmetrical 25-Level cascaded H-bridge gives voltage THD of 5.49% where as the current gives 2.60%. The above results clearly indicate that as the output Voltage levels are increased, the THD of the system decreases

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